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02/20/02

PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10081344	FILING DATE 02/20/2002	CLASS 327	SUBCLASS	GAU 2816	EXAMINER ME - >
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**\*\*APPLICANTS:** Mashimo Akira;

**\*\*CONTINUING DATA VERIFIED:**

**\*\* FOREIGN APPLICATIONS VERIFIED:**  
 JAPAN 2001-044223 02/20/2001  
 JAPAN 2001-333102 10/30/2001

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no Verified and Acknowledged Examiners's initials		ATTORNEY DOCKET NO MM4521
TITLE : Signal processing circuit integrating pulse widths of an input pulse signal according to polarities		

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L/Rev. 12-94

<b>NOTICE OF ALLOWANCE MAILED</b>		Assistant Examiner	<b>CLAIMS ALLOWED</b>	
			Total Claims	Print Claim for O.G.
<b>ISSUE FEE</b>		Primary Examiner	<b>DRAWING</b>	
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg.
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>PREPARED FOR ISSUE</b> <b>WARNING:</b> The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	Application Examiner	

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